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13. ABSTRACT *(Maximum 200 words)*

This research project corresponds to one of the first comprehensive studies in multi-channel switching. Assuming a broadband communication environment using ATM technology, this work investigates the fundamental characteristics of multi-channel switching. Potential benefits of multi-channel switching over traditional point-to-point switching have been identified. A clear theoretical foundation is being developed and theoretical limits on various performance measures are being investigated.

Attainable performance objectives in multi-channel switches under the current state of technology are being determined, and implementable multi-channel switching architectures that satisfy the objectives are being formulated. A comprehensive study of the efficacy of the proposed architectures is being conducted under varying traffic and network conditions. One of the main tasks in this project is to exhibit the feasibility of the proposed switching architectures via prototyping.

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FINAL REPORT ON MULTI-CHANNEL SWITCHING IN OPTICAL FIBER NETWORKS

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1. INTRODUCTION

On September 20, 1993, ARPA awarded a grant entitled, "Multi-Channel Switching in Optical Fiber Networks," to Washington University with Paul S. Min as the principal investigator. This grant is part of the 1993 Research Initiation Program by DoD, and Lt. Col. James Crowley was then the technical coordinator at ARPA. Louisiana State University is included in the grant as a subcontracting institution with Manju V. Hegde as the principal investigator.

In Section 2, a brief description of the project is given. The results accomplished during three years of the project duration (i.e., 9/20/93 - 9/19/96) are summarized in Section 3. Section 4 contains the list of the publications that we generated during the project period. Below is the research plan which was stated in Section 4 (pp. 13-14) of the original proposal (dated January 12, 1993).

- Year 1 (9/20/93 - 9/19/94):
  - Theoretical formulation for multi-channel switching (WU and L.S.U.).
  - Validation of benefits in broadband network (L.S.U.).
  - Characterization of generic multi-channel switching functions (WU).
  - Formulation of performance objective (WU).
  - Comprehensive study of various ATM architectures (WU and L.S.U.).
- Year 2 (9/20/94 - 9/19/95):
  - Theoretical limits on performance indices (WU and L.S.U.).

- Efficacy of multi-channel switching with respect to point-to-point switching (L.S.U.).

- Formulation of (nearly) optimal architectures (WU and L.S.U.).

- Feasibility study under current state of technology (WU).

- Formulation of implementable architectures (WU).

- Efficiency study with respect to the optimality (L.S.U.).

- Efficiency study with respect to the known ATM switches (L.S.U.).

- Prototyping (WU).

• Year 3 (9/20/95 - 9/19/96):

- Prototyping (WU).

- A comprehensive study under varying traffic and network conditions (WU and L.S.U.).

- Compatibility validation using the test ATM network in St. Louis (WU and L.S.U.).

2. BRIEF DESCRIPTION OF PROJECT

Asynchronous Transfer Mode (ATM) is a high bandwidth, low delay, packet like switching and multiplexing technique that supports integrated access for a wide variety of applications. In 1988, ATM was recommended by CCITT as the target transfer mode solution for implementing broadband communication networks. ATM is a connection-oriented service which yields in-order packet arrivals, and is intended to provide high performance communication services.

While strong consensus exists on ATM within the broadband community, some difficult technical challenges lie ahead. One such problem, which this proposal addresses, is the development of a switching methodology that can support the very high bandwidth transmission associated with lightwave technology. The transmission rate over optical fibers has reached tens of giga bits per second and is likely to increase fast in the coming years. On the other hand, the processing speed of electronic switches remains substantially slower. Such a mismatch between the two quantities creates a natural bottleneck at the switching nodes in the network.

Multi-channel switches have been proposed as a means of alleviating the processing speed constraint of electronic switches in the broadband networks. We summarize below some of the benefits realizable by multi-channel switches.

Multi-channel switches can provide higher performance (e.g., throughput, blocking probability, delay) by exploiting the concept of *trunk grouping*. Instead of being routed to a specific output channel, a packet is routed to any channel belonging to an appropriate trunk group. In ATM, a session is established by the assignment of a virtual circuit. The virtual circuit is defined in terms of a specific channel between the two end points of the session. However, many of the

benefits associated with connection-oriented services do not require that the connection be specified at the channel level; it is sufficient to specify the path of the connection, not the specific channel within the path. This implies, among other things, that a packet can be routed to any output channel of a switch within a group of outputs, provided that it eventually leads to the same end point. We note that any interswitch connection is likely to be in the range of multiple giga bits per second, e.g., 2.4 giga bits per second via an OC48 connection of SONET. This corresponds to a number of ATM channels at 155 mega bits per second or 620 mega bits per second, and a trunk group may be defined as a collection of these channels transmitted over a single optical fiber.

As the demand for new applications soars, greater variability in bandwidth and traffic characteristics (e.g., session duration, burstiness) is expected. The advantages of *statistically sharing* a higher channel capacity under such conditions are well known. For example, it increases the link efficiency by reducing the burstiness in the incoming traffic. Bit pipes of higher rates are formed which allow a number of applications to share bandwidth by dynamically allocating time slots. Assuming that the exogenous traffic intensity per channel is fixed, a larger trunk group size is less likely to incur blocking for a single ATM cell, for a burst of cells, or for a request for setting up a new session. Similarly, other performance measures such as cell delay, probability of buffer overflow, and congestion would improve when multiple channels are grouped together as a single resource.

Another important benefit of multi-channel switching is the ability to provide *super-rate switching*. Applications requiring peak rates greater than a single ATM channel capacity would suffer high cell loss probability unless these applications can be assigned over multiple channels.

Trunk grouping would be a natural way to deal with such a problem. In reality, a trunk group may correspond to a single fiber operating at an extremely high rate, and multi-channel switches can provide a means of transporting this bit pipe across broadband networks without requiring complex multiplexing/demultiplexing functions at each switching node.

A significant benefit could come from reduction in the *control complexity*. The overall control of multi-channel switches ought to be simpler than that of point-to-point switches, since a packet is routed to any channel within a large group (rather than to a specific channel which is a stricter routing constraint). As a result, it is likely to require fewer searches in order to set up a virtual path within the available paths. So, at least in theory, the complexity of the control algorithm can be made lower which would result in yet greater gain in the throughput. However, we note that the multi-channel switches proposed thus far suffer from higher (than point-to-point switches) levels of control complexity, lower throughput, and/or inflexibility in the grouping of trunks. One of the main goals in our work is to develop methodologies for multi-channel switching that are efficient and deal effectively with these deficiencies.

Lastly, *cross-point complexity* in multi-channel switches can be low. We illuminate such a possibility: Given N inputs and N outputs, let us construct a switch that provides at least one path between every pair of input and output channels. A switch based on the banyan network would require $\log_2 N$ interconnected stages, each consisting of $\frac{N}{2}$ $2X2$ switching elements. On the other hand, if the requirement is changed such that each input is connected to any of the outputs in the same group, then the number of stages of the same switch can be less. Assume, for example, that two outputs of the individual switching elements at the last stage of the Banyan network are bundled into a group such that there are $\frac{N}{2}$ trunk groups of two channels each. Then

the switching function at the last stage is unnecessary since ATM cells arriving at these switching elements can be switched to any of the two outputs. In this case, the banyan network with $\log_2 N - 1$ stages would suffice. We can continue this argument to show that for $2^{-r}N$ trunk groups ($r \leq \log_2 N$), the resulting multi-channel switch requires r stages less than the original point-to-point switch.

This research project corresponds to one of the first comprehensive studies in multi-channel switching. Assuming a broadband communication environment using ATM technology, this work investigates the fundamental characteristics of multi-channel switching. Potential benefits of multi-channel switching over traditional point-to-point switching have been identified. A clear theoretical foundation is being developed and theoretical limits on various performance measures are being investigated.

Attainable performance objectives in multi-channel switches under the current state of technology are being determined, and implementable multi-channel switching architectures that satisfy the objectives are being formulated. A comprehensive study on the efficacy of the proposed architectures is being conducted under varying traffic and network conditions. One of the main tasks in this project is to exhibit the feasibility of the proposed switching architectures via prototyping.

At the conclusion of this project, we hope to have ignited interest in multi-channel switching within the broadband communication community by suggesting methods to alleviate the bottleneck in the processing speed of electronic switches and by proposing simple, inexpensive switching architectures that can support very high bandwidth in ATM networks.

3. SUMMARY OF ACCOMPLISHMENTS: SEPTEMBER 1993 – SEPTEMBER 1996

During Year 1 of this project, we have concentrated on a number of analytical studies which investigate various issues in controlling and managing broadband traffic under multi-channel switching. There have been many fruitful developments in this effort, and we gained a comprehensive understanding on the impact of multi-channel switching on the broadband network. Much of our analytical effort have been documented in a substantial number of publications we compiled, which we list in Section 4.

Year 2 of this project had been an extremely challenging period. A significant fraction of our funding and man power has been consumed by prototyping hardware and software. One of the important goals of the project is to demonstrate the conceptual advances we made to the broadband community via prototyping, and in order to accomplish this goal within the project period, it became necessary for us to commence the implementation phase very early on in Year 2. At the same time, we have intensified our efforts for the analytical studies we had planned to conduct.

Based on the experiences and the analytical insights we have gained during the first two years of the project, we proceeded Year 3 with a higher level of intensity and innovative ideas. Specifically we have focused in completing one of the main goals of this project, namely developing a prototype of the WUMCS switch. We were also occupied with developing all necessary software and completing design documents that make our prototype more useful for the practitioners.

At the conclusion of this project, we are proud to report that we have successfully completed all the goals in the project, including successful implementation of the WUMCS prototype which has been tested in a laboratory for its full functionality. In addition to all the fundamental insights we gained in multi-channel switching in fiber optic networks, we have a collection of hardware and software which are relevant and practical, and are viewed as fundamental innovation by the practitioners in the field.

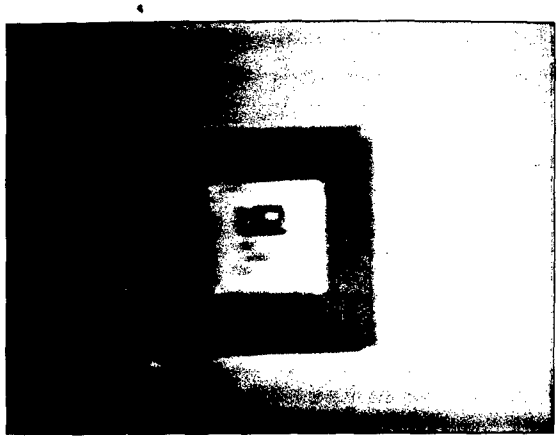

Figure. CN/RN Switch IC for WUMCS

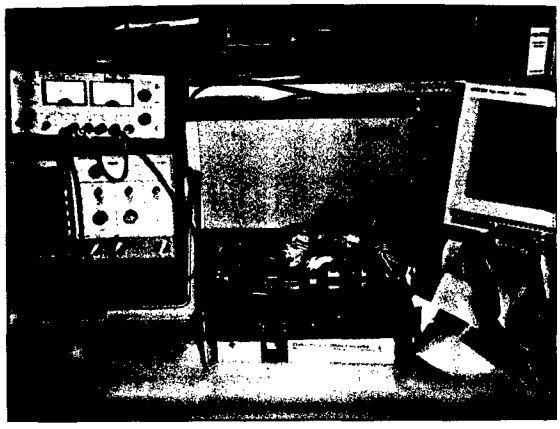

Figure. Evaluation Board for Testing CN/RN Switch IC

We now summarize some of the tangible accomplishments associated with this project.

- The following U.S. Patents have been approved and issued:
  - "Nonblocking Multi-Channel Switching with Multicasting Capability," U.S. Patent No. 5,440,549, 35 claims.
  - "Integrable Low Complexity Multi-Channel Switch," U.S. Patent No. 5,526,352, 24 claims.
- The following patent applications have been filed:
  - Patent Treaty Country Protection filed for "Multi-Channel Switch on a Single Chip" in 15 countries.

- U.S. Patent Application filed for "Network Design Algorithm Using Shadow Prices for Adaptively Routed Networks."

• We have been instrumental in the following special events:

- We will organize several broadband-related special sessions at *International Symposium on Integrated Network Management* which will be held in San Diego in April 1997.
- We will organize one broadband-related special session at *Conference on Information Sciences* and *Systems*, which will be held in Baltimore in March 1997.
- We edited a special issue on *Routing in Broadband Networks* for *Journal of Network and Systems Management.* Two volumes of this issue have been published in December 1995 and in June 1996.
- We organized several broadband-related special sessions at *International Symposium on Integrated Network Management* which was held in Santa Barbara in April 1995.
- We helped organizing the *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing,* which was held in St. Louis in April 1995.

• We gave the following invited seminars:

- A presentation at the IEEE Information Theory Workshop in St. Louis on April 19, 1995. We illustrated various architectural issues in broadband packet switching.
- A tutorial lecture on ATM switching at Japan Radio Company in Mitaka, Japan on June 21, 1995.
- Two formal presentations at Washington University on broadband communication, on November 18, 1994 and on September 12, 1995.

- We developed the following graduate level courses at Washington University:

  "Signaling and Control of Communications Networks," EE 593 / CS 593.

  "Queueing Systems and Discrete Stochastic Processes," EE 536 / CS 567.

  "Introduction to Data Networks," EE 530.

  "Computer/Communications System Analysis," EE 558 / CS 558.

- We produced the following degrees which are associated with the project:

  - 4 DSc. degrees granted.

  - 7 MS. degrees granted.

  - 6 BS. degrees granted.

  - Additional 3 DSc. degrees will be granted as a result of the project.

  - Additional 2 MS. degrees will be granted as a result of the project.

  - Additional 2 BS. degrees will be granted as a result of the project.

- The following is our publications activity:

  - 17 journal papers accepted or published.

  - 37 conference papers published.

  - 6 technical reports published.

We are very proud of our progress in this project. We have made significant advances in both analytical work and prototyping activities. We give a brief summary of our accomplishments below.

On Theoretical Limits on Performance Indices

We have conducted a series of performance studies on the maximum throughput of multi-channel switches. In [42], for example, we have developed analytical methods for each of the

popular buffering schemes, i.e., input buffering, output buffering, shared buffering, and bufferless architecture. As a result of [42], we are able to tradeoff various switching complexities factors such as buffer sizes, pin counts, gate counts, and fabric clock speed under the consideration of throughput and delay.

We have also conducted similar studies for the multicast copy network. In [18], [32] and [38], we derived the throughput, delay, and cell loss characteristics for the nonblocking copy networks that can maintain the cell sequence. In [40], similar analysis has been done for an architecture that distributes the copying function to individual switching elements, and thus is highly scalable with respect to the number of input channels.

In [35], we developed a framework for the throughput of a network as a whole. We borrowed a concept from the operations research, which is known as shadow prices and were able to formulate an optimization problem for the network with the total throughput as the objective function. We derived the shadow prices for the optimization with respect to exogenous traffic variables, and from them, we determined the total throughput of the network. The particular example in [35] is for single rate homogeneous networks, but the same framework can be applied to multirate ATM networks albeit with a higher computational complexity.

On Efficacy of Multi-Channel Switching

A significant amount of work has been done in [1]. This along with [2] and [6] showed conclusively that multi-channel switching realizes the queueing economies of scale, which is critical in increasing the utilization and the performance of switching devices. We demonstrated in [1], [2], and [6] that with multi-channel switching, the throughput can be increased dramatically under a variety of cell loss threshold values.

In [32],[38],[43], and [44], we carried out further performance studies to quantify the efficacy of multi-channel switching.

On Formulation of (Nearly) Optimal Architectures

In [28], we presented the results of our design effort for a highly efficient multi-channel switch. The resulting architecture can provide extremely high performance through channel grouping, multicasting, multi-rate switching, and super-rate switching. The architecture also eliminates needs for any resequencing circuitry which may be complex in hardware and control control algorithm[3]. The architecture is also able to shape the arriving traffic patterns in a flexible manner.

The architecture, which has been implemented as the Washington University Multi-Channel Switch (WUMCS), is one of the first multi-channel switches that guarantees cell sequencing integrity without the use of resequencing circuits [3].

On Formulation of Implementable Architectures

Based on the original ideas developed in [2], we have formulated an architecture that displays many of the ideal characteristics of ATM switching. Specifically, we have sought to achieve single chip integrability, scalability to large input channels, low and stable internal fabric clock frequency, low crosspoint complexity, and low control complexity. We have documented an architecture that satisfies these characteristics in [9] [10] [28].

The single integrated circuitry that we developed realizes all but simple table translation functions of the WUMCS with 16 input-output pairs [30]. The architecture is so simple and efficient that we were able to utilize conservative technology (i.e., 0.6 micron CMOS with 208-pin

IC package). The resulting circuitry runs at only 27 Mhz internal clock frequency, which is much slower than most ATM switching architectures.

This is an indication that what we have developed is a highly efficient switching system and that if and when we decide to use more aggressive technology or higher internal clock frequencies, we can indeed develop ATM multi-channel switches with much larger numbers of input-output pairs runing at much higher channel speeds. To the best of our knowledge, this is the first fully implemented architecture for multi-channel switching which guarantees time sequence among the cells that belong to a single traffic stream and that traverse the network via different physical channels. Our architecture can switch large bit rates (e.g., > giga bits per second) by grouping a number of physical channels together.

On Feasibility Study under Current State of Technology

The feasibility of the proposed architecture has been verified and documented in [28] and [30]. We have completed all the schematic designs for the copy network/routing network IC and these designs have been verified physically as well as logically using the electrical delay characteristics provided by our fabrication vendor, United Silicon Structure located in San Jose, CA.

We have also used the computer aided design tool developed by Mentor Graphics Inc. in verifying the correctness of our design in terms of logical and timing tests. For the logical verification, we developed VHDL models for all the components in the WUMCS including the interface circuitry to the switch controller. We conducted the timing tests in terms of the maximum delay bounds and also using a statistical simulator.

During the period of December 20, 1994 - January 4, 1995, we held a series of design review meetings. During the design review meetings, we discussed many of the designs in detail

and verified the consistency amongst subcomponents of the switching system, which are designed by different individuals. The last design review session on January 4 was open to the public, and we solicited inputs from various experts in the broadband switching and high speed electronics fields. All together about 25 people attended this open design review meeting, representing a dozen different organizations. The content of the design review are summarized in [29] in a viewgraph form.

On Efficiency Study with Respect to Optimality

As a result of the numerous performance studies we conducted, we are able to compare the performance of our architecture with the theoretically suggested optimum. For example, in [42], we derived the maximum throughput for all known buffering schemes under a variety of buffer sizes. These results can be compared with the performance of the architecture being implemented as given in [2] and [32].

From the comparison, relative efficiency of our architecture can be seen with respect to the optimal performance. Also as a result of our efforts in [28], we can bring other factors such as the design complexity and production cost into the comparison. We are now able to make an intelligent decision in selecting an architecture and its configuration based on practical as well as theoretical considerations.

On Efficiency Study with Respect to Known ATM Switches

We have carefully studied the performance of other ATM switch architectures. For example, in [33], [40], and [41], we considered internally buffered switches, and in [4], [6], and [51] we considered the switches based on deflection routing. These classes of switches are known to

reduce the electronic processing overhead.

We have presented the results of our investigation at the *IEEE Information Theory Workshop* in St. Louis which we helped organizing. We presented several alternatives to our current design in consideration of the possible increases in the number of channels and the speed of each channel.

In [19], we studied the effects of different copying policies in the throughput, and a similar study for slot splitting was conducted in [22].

On Prototyping

The prototyping activity has been in full swing for the most of Year 3. The prototype has been completed and we received the working parts that have been verified in September 1996. We then spent the next three months verifying the correctness of the ICs.

We have completed all the circuit designs at the IC level and at the board level. This includes CNRN IC design, all table translators, interface cards to the switch controller, and a variety of test circuitry.

We developed a clock recovery scheme that can be operated at up to 1.2 Gbps transmission speed. Such a scheme is trickly to devise when there are multiple switching devices operating at varying channel speeds.

We have developed a method of distributing the internal fabric clock to more than 8,000 components. This too had been a difficult task to accomplish due to the large number of clocked elements. We were able to devise a scheme that can tolerate up to 1.5 nano seconds of clock skew amongst the 5 clock trees needed to drive the CNRN IC.

We also have developed transmitter/receiver link card for SONET. Currently all the design and testing tasks have been done for SONET OC3 interace and a work is under way to develop a SONET OC12c interface capability.

It should be noted that the prototyping effort includes not only the hardware design, but also the development of software protocols, testing and simulation tools, and demonstration systems.

4. LIST OF PUBLICATIONS DURING 9/93 – 9/96

[1] **"Multi-Channel Switching in Broadband ATM Networks,"** *Doctoral Thesis* by H. Saidi, Department of Electrical Engineering, Washington University, February 3, 1994.

[2] **"A Nonblocking Architecture for Broadband Multi-Channel Switching,"** *IEEE Transactions on Networking*, April 1995.

[3] **"Guaranteed Cell Sequence in Nonblocking Multi-Channel Switching,"** *IEEE INFOCOM 94*, Toronto, June 1994.

[4] **"Control of Packet Flow in Statistical Data Forks,"** *ICC '94*, New Orleans, May 1994.

[5] **"Nonblocking Multi-Channel Switching In ATM Networks,"** *ICC '94*, New Orleans, May 1994.

[6] **"A New Structural Property of Statistical Data Fork,"** *IEEE Transactions on Networking*, June 1995.

[7] **"Analysis of Nonblocking Copy Networks with Shared Buffering,"** *International Symposium on Information Theory*, Norway, June 1994.

[8] **"Internal Buffering in Banyan Based Copy Networks,"** *Conference on Information Sciences* and *Systems*, Princeton, March 1994.

[9] **"Washington University Multi-Channel Switch (WUMCS): Functional Requirement Document,"** *Technical Report*, Department of Electrical Engineering, Washington University, December 1993.

[10] **"Washington University Multi-Channel Switch (WUMCS): System Architecture Document,"** *Technical Report*, Department of Electrical Engineering, Washington University, January 1995.

[11] **"Analysis of State Dependent Routing in Circuit Switched Networks."** *Doctoral Thesis* by H. Rayes, Department of Electrical Engineering, Washington University, January 1994.

[12] **"State Dependent Routing: Traffic Dynamics and Performance Benefits,"** *Journal of Network* and *System Management*, June 1994.

[13] **"Analysis and Development of Routing Schemes for Multi-Rate, Multi-Point Traffic,"** *Conference on Information Sciences* and *Systems*, Princeton, March 1994.

[14] **"Shadow Prices for State Dependent Routing,"** *Conference on Information Sciences* and *Systems*, Princeton, March 1994.

[15] **"Estimation of Exogenous Traffic Based on Link Measurement of Circuit-Switched Networks."** *IEEE Transactions on Communications*, December 1995.

[16] **"Capacity Expansion in State Dependent Routing Schemes,"** *Conference on Information Sciences* and *Systems*, Princeton, March 1994.

[17] **"Real Time Traffic Estimation in Circuit-Switched Networks,"** *14th International Teletraffic Congress*, France, June 1994.

[18] **"Multi-Channel Copy Networks: Architecture, Performance Model, Fairness, and Cell Sequencing."** *IEEE INFOCOM 95*, Boston, April 1995.

[19] **"Fanout Splitting in Nonblocking Copy Networks with Shared Buffering,"**

Thirty Third Annual Allerton Conference, October 1995.

[20] **"Maximum Throughput of Banyan-Based Copy Networks with Internal Buffers,"** submitted to *IEEE Transactions on Communications*.

[21] **"Washington University Multi-Channel Switch (WUMCS): CNRN Functional Specifications,"** *Technical Report*, Department of Electrical Engineering, Washington University, September 1994.

[22] **"Slot Splitting: A New Schedule for Multi-cast Mult-rate Traffic,"** *3rd International Conference on Computer Communications* and *Networks*, San Francisco, September 1994.

[23] **"Scheduling Multi-Rate Traffic in Time-Multiplex Switches,"** *International Symposium on Information Theory*, Norway, June 1994.

[24] **"Fault Tolerance Design of Feedforward Networks,"** *World Congress on Neural Networks*, San Diego, June 1994.

[25] **"Fault Tolerant Radial Basis Function Networks,"** *World Congress on Neural Networks*, San Diego, June 1994.

[26] **"Learning Algorithm for Fault Tolerance in Radial Basis Function Networks,"** *1994 Midwest Symposium on Circuits* and *Systems*, Lafayette, August 1994.

[27] **"Analysis and Development of Routing Policies in Multi-Rate, Multi-Point Networks,"** *Master Thesis* by A. Maunder, Department of Electrical Engineering, Washington University, April 1994.

[28] **"Washington University Multi-Channel Switch (WUMCS): CNRN Trap/Group/Route**

Paradigm Specification and Design Document," *Technical Report*, Department of Electrical Engineering, Washington University, December 1994.

[29] **"Washington University Multi-Channel Switch (WUMCS): Formal Design Review,"** *Technical Report*, Department of Electrical Engineering, Washington University, January 1995.

[30] **"Washington University Multi-Channel Switch (WUMCS): Design Schematics,"** *Technical Report*, Department of Electrical Engineering, Washington University, January 1995.

[31] **"Application of Shadow Price in Capacity Expansion of State Dependent Routing,"** *Journal of Network and Systems Management*, March 1996.

[32] **"Nonblocking Copy Networks in Multi-Channel Switching,"** *IEEE Transactions on Networking*, December 1995.

[33] **"Analysis of Banyan Based Copy Networks with Internal Buffering,"** *Journal of High Speed Networks*, December 1995.

[34] **"Analysis of Routing Policies in Broadband Networks,"** *Canadian Journal of Electrical and Computer Engineering, Special Issue on Planning and Designing of Broadband Networks*, July 1995.

[35] **"Shadow Prices for Least Loaded Routing and Aggregated Least Busy Alternate Routing,"** *IEEE Transactions on Networking*, December 1996.

[36] **"Telecommunications Network Management into the 21st Century,"** *IEEE Communications*, July 1994.

[37] **"Capacity Expansion of Least Busy Alternate Routing with Shadow Price,"** *GLOBECOM 95*, Singapore, November 1995.

[38] **"Architecture and Performance of Nonblocking Copy Networks with Multi-Channel Switching,"** *APCC 95*, Osaka, Japan, June 1995.

[39] **"Routing for Multi-Rate Traffic with Multiple Qualities of Service,"** *Third International Conference on Computer Communications* and *Networks*, San Francisco, September 1994.

[40] **"Throughput and Delay for Copy Networks with Internal Buffers,"** *33rd Annual Allerton Conference*, October 1995.

[41] **"Analysis of Packet Movements in Internally Buffered Copy Networks,"** *Third ORSA Telecommunications Conference*, Boca Raton, Florida, March 1995.

[42] **"Performance Benefits of Multi-Channel Switching,"** *32nd Annual Allerton Conference*, September 1994.

[43] **"Shared Buffering in Nonblocking Copy Networks,"** *1994 IEEE International Symposium on Information Theory*, June 1994.

[44] **"Non Blocking Multi-Channel Switching,"** *31st Annual Allerton Conference*, September 1993.

[45] **"Noise Modeling Effects in Redundant Synchronizers,"** *IEEE Transactions on Computers*, December 1993.

[46] **"Convolutional Coding for Finite-State Channels,"** *IEEE Transactions on Communications*, June 1994.

[47] **"Conditional Connectivity Measures for Large Multiprocessor Systems,"** *IEEE Transactions on Computers*, January 1994.

[48] **"DPCM Encoding of Regenerative Composite Processes,"** *IEEE Transactions on Information Theory*, January 1994.

[49] **"On The Capacity Of Constrained Connectivity Hopfield Neural Networks,"** *Neural Parallel & Scientific Computation*, March 1994.

[50] **"Flexible Learning Rules For Neural Networks,"** *Neural Parallel & Scientific Computation*, December 1994.

[51] **"The Deflecting Multicast Switch,"** *Fourth International Conference on Computer Communications and Networks*, September 1995.

[52] **"Scheduling multi-rate traffic in a time-multiplex switch,"** *IEEE International Symposium on Information Theory*, July 1994.

[53] **"Design of fault-tolerant feedforward neural networks,"** *Proceedings of the World Congress on Neural Networks,* June 1994.

[54] **"Genetic Algorithm Applications to Fault-Tolerant Neural Network Design,"** *Proceedings of the World Congress on Neural Networks,* June 1994.

[55] **"Slot Splitting: A New Schedule for Multi-cast, Multi-rate Traffic,"** *Proceedings of the Third International Conference on Computer Communications and Networks,* September 1994.

[56] **The Deflecting Multicast Switch,"** *Proceedings of the Fourth International Conference on*

Computer Communications and Networks, September 1995.

[57] **"Shadow Prices for Modified Least Loaded Routing,"** *Proceedings of the Twenty-Eighth Southeastern Symposium on System Theory,* April 1996.

[58] **"A Multiple Shared Memory Switch,"** *Proceedings of the Twenty-Eighth Southeastern Symposium on System Theory,* April 1996.

[59] **"Use of Shadow Prices in Wireless Networks,"** *Proceedings of the Third International Telecommunications Symposium,* October 1996.

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